AMENDMENTS TO DRAWINGS:

The attached drawing sheet includes changes to Fig. 9. This sheet, replaces the original sheet including Fig. 9. In Figure 9, the Fout connection to PFD2 (205) is changed to first go through FDW (225) prior to being routed to PFD2 (205).

REMARKS

A. Drawing Amendments:

The correction to Fig. 9 makes Fig. 9 consistent with its description provided in paragraph 38 of the specification. Specifically, lines 2-6 of paragraph 38 state that,

> "output timing signal **Fout** is an input to frequency divider circuit **225**. The input reference signal **Fref** and the frequency divided signal from the frequency divider circuit 225 are applied to a separate phase-frequency detector **205**".

From the above excerpt, it is clear that in Fig. 9, signal Fout should have been shown inputted to frequency divider circuit 225, and that the output from frequency divider circuit 225 (i.e. the resultant "frequency divided signal from the frequency divider circuit 225) is applied to the second phase-frequency detector 205.

B. Specification Amendments:

The change to paragraph [0038] makes it more consistent with Fig. 9. That is, Fig. 9, as originally filed, clearly shows that reference signal F_{ref} is applied to frequency divider 225, and that the output from frequency divider 225 is applied to second phase-frequency detector 205. By contrast, paragraph 38 as originally filed, stated that input reference signal F_{ref} is applied directly to second phase-frequency detector 205. The amendment to Fig. 38 makes the description of input reference signal F_{ref} consistent with Fig. 9, as originally file. Also for consistency with original Fig. 9, paragraph [0038] is amended to state that reference signal F_{ref} is applied to frequency divider 225, and that the frequency-divided F_{ref} signal outputted from frequency divider 225 is applied to second phase-frequency detector 205. This correction is consistent with the remainder of paragraph 38, where it is explained that, "[t]he separate phase-frequency detector 205 functions at a different frequency than the phase-frequency detector 10 of Fig. 8". As it is known in the art, the frequency of

operation of the phase-frequency detector, in the present case, is determined by its inputs.

C. Claim Amendments:

Claims 1, 4-15, 19, 22-24, 37-47, and 57-60 are presented for prosecution. Claims 1, 7, 10, 11, 12, and 19 are currently amended. Claims 2, 3, 16-18, 20, 21, 25-36, and 48-56 are cancelled. Claims 57-60 are new.

Clams 37-47 are allowed. Applicants thank the Examiner for allowance of these claims.

Claims 3, 12, and 21 were objected as being dependent upon a rejected claim, but would be allowable if rewritten in independent form. Applicants thank the Examiner and have incorporated all the limitations of claim 3 into its base claim 1, which is now believed to be in condition for allowance. Claim 3 is subsequently cancelled. Claims 4-6, which depend from claim 1, are believed to be in condition for allowance based at least on the allowability of their base claim 1.

Claim 12 is rewritten in independent form including all the limitations of its base claim 10, and is believed to now be in condition for allowance.

All the limitations of claim 21 have been incorporated into its base claim 19, which is now believed to be in condition for allowance. Claim 21 is subsequently cancelled. Claims 22-24, which depend from claim 19, are believed to be in condition for allowance based at least on the allowability of their base claim 19.

Claim 7, as originally filed already recited the phase lock loop as being separate and distinct from the claimed lock detection circuit, but the claim rejections appeared to ignore this distinction. That is, the claim 7 recited that he claimed lock detection circuit has its own phase-frequency detector (separate from any phase-frequency detector in the phase lock loop). However the claim rejections appear to construe the phase-frequency detector of a phase-lock loop as being part of the presently claimed lock detection circuit. To remove any unintended ambiguity, claims 7 has been amended to more clearly state that the

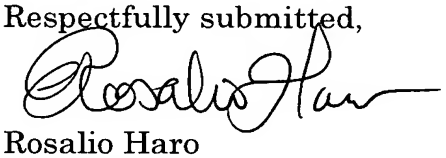
lock detection circuit is different and separate from the phase lock loop, and thus has its own internal components. Specifically, claim 7 is amended to more clearly recite that the claimed lock detection circuit has its own, second phase-frequency detector monitoring the phase lock loop, and that this second phase-frequency detector is separate from a first phase-frequency detector internal to the phase lock loop. None of the cited prior art teach or suggest such a structure.

New claims 57 and 58 describe the use of a frequency divider to generate the inputs to the second phase-frequency detector of the lock detection circuit of claim 7, as show at least in current Fig. 9 of the present invention.

Claim 10 is amended for similar reasons as claim 7. Similarly, new claims 59 and 60 describe the use of a frequency divider to generate the inputs to the second phase-frequency detector of the lock detection circuit of claim 10, as show at least in current Fig. 9 of the present invention.

In view of the foregoing amendments and remarks, Applicants respectfully request favorable reconsideration of the present application.

Respectfully submitted,



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